OverMOS

OverMOS: Overdepleted CMOS Monolithic Active Pixel Sensors (MAPS) for very high radiation hardness and speed

Project outline

As originally proposed by one of us [ref], CMOS Monolithic Active Pixel Sensors (MAPS) are now starting to be used in particle physics experiments. A MAPS detector is already installed in STAR at RHIC [ref] and Alice at LHC is now going to build their upgraded tracker with CMOS MAPS[ref]. This will be built using the INMAPS process that the STFC team developed under the CfI programme a few years ago [ref]. The INMAPS process allows MAPS pixels to have the same complexity of electronics as found in hybrid sensors without compromising the charge collection performance. In order to make MAPS the solution of choice for most if not all experiments, we now propose to take on the next and ultimate challenge, i.e. to achieve radiation hardness levels as required by the extremely harsh environments found in the other LHC experiments. A very rad-hard MAPS will also provide benefit in terms of imaging speed. Several areas across STFC science and impact will benefit from this work.

CMOS MAPS designed in an INMAPS process have been proven to be radiation hard for the level of radiation required for Alice at LHC, i.e. MRad and … n cm-2 equivalent [ref TDR]. As already pioneered by the STFC team within the CfI programme, high resistivity substrates, i.e. rho >~ 1k Ohm cm, are used in this case. Even with the small voltages normally available in CMOS, i.e. a few V, a significant part of the substrate is depleted (Figure 1). An electric field is present in the depletion region, thus speeding up charge collection and reducing the spread of charge between several pixels. This in turn is beneficial for the detection efficiency as the average signal over noise ratio for a signal pixel is increased. It is also beneficial for radiation hardness, as the reduced charge collection time means the sensors is less affected by the reduction of the minority carrier collection time due to the lattice damage generated by Non Ionising Energy Loss (NIEL).

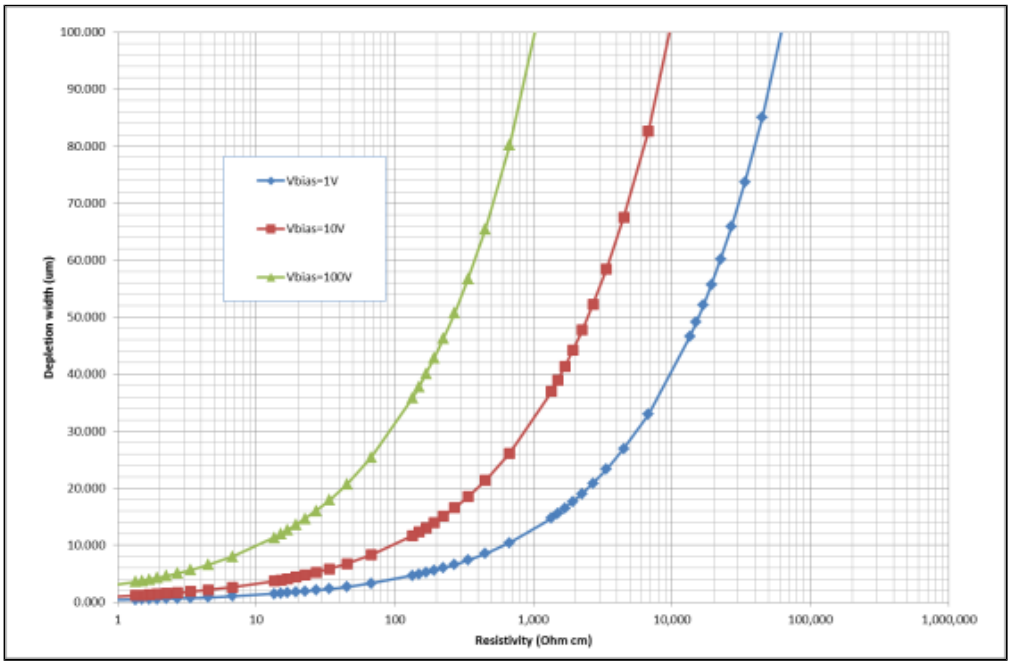


Figure 1. Calculated depletion width as a function of the substrate resistivity for different values of the applied bias voltage.

In order to cope with the higher level of irradiation found in Atlas and CMS, one has to apply higher bias voltages in order to counteract two effects:

- Radiation induced defects behave like P-type impurity, thus effectively reducing the substrate doping
- The minority carrier lifetime continuously reduces, thus requiring faster collection times if one wants to collect enough signal

In order to be able to apply biasing voltages higher than the standard CMOS voltages, special biasing scheme needs to be designed. We have already identified two very promising biasing schemes:

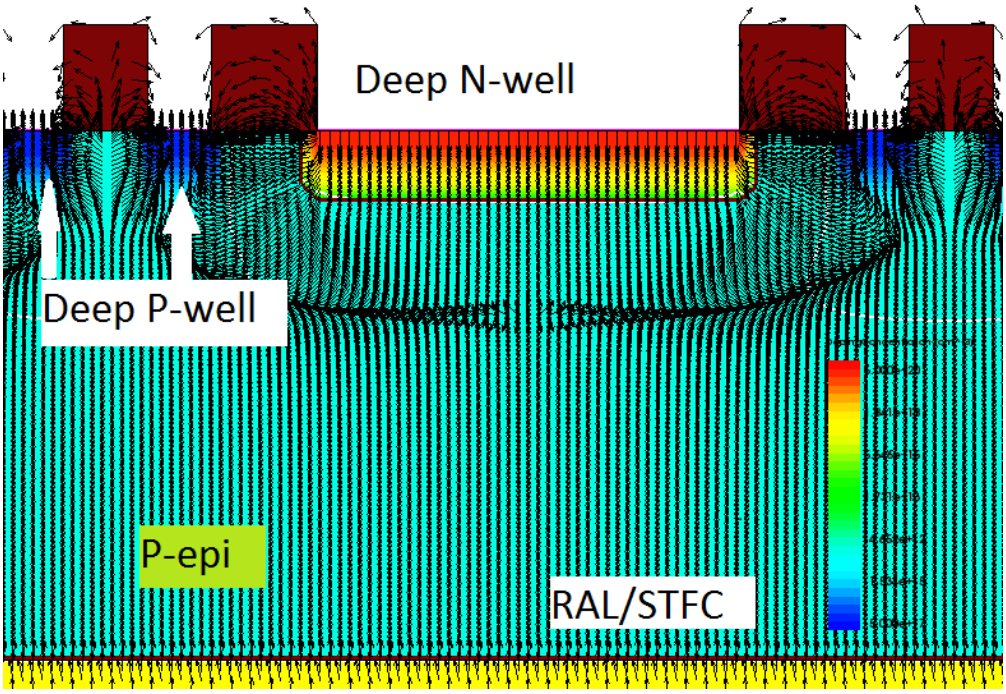
- Lateral depletion
- Double, back-to-back junction depletion

While the general concepts for these two schemes are not new, their application in CMOS is very limited. We have already identified a European Foundry, Espros-EPC, which has a similar scheme. Sample diodes have been obtained and will be tested during this work. However, the main part of this proposal will be the design of our own biasing structure as well as the manufacturing and the characterisation of test structures based on our own concept. Some simple pixel array based on this concept will also be designed. The reason why we do not want to rely to the Espros concept is twofold:

- The basic substrate used by Espros is N-type, so it should invert to P-type at high level of irradiation, thus probably invalidating their biasing scheme.
- Even if the Espros concept was successful, and it will work for sure at least up to a certain level of irradiation, this is proprietary and it will then tie us in on a very risky single vendor scheme. By developing our own concept, we should be able to apply it to different foundries, thus allowing us to choose the best one for a given application.

The bulk of the work will consist in the device simulation of the biasing structures and their design in a deep submicron CMOS technology. We are currently exploring three different vendors: Espros-Epc, LFoundry as well as TowerJazz. Because of our long standing relationships with TowerJazz, with which we have developed the INMAPS process, as well as CCD in CMOS for the ultra-high speed camera Kirana and low dark current Single Photon Avalanche Detectors (SPAD), they represent our baseline choice, although we will continue to explore the possibility to use other foundries if better suited for performance or cost. In any case, we plan to develop a biasing scheme that will be independent from the foundry choice. We will also design a pixel structure with a front-end as close as possible to what require by LHC experiments. In order to achieve this goal with the limited amount of money and time, we propose to use the PImMS pixel as a starting design. It has already been demonstrated to work at 40 MHz with low noise, so it already provides some of the performance required in LHC experiments.

While the ultimate target could be a CMOS MAPS suitable for vertex at Atlas and CMS, within the limited budget and timescale of this programme, we would like to demonstrate that the structure is capable of sustain levels of radiation as seen in the Atlas and CMS tracker, or at least be close to it so that a second iteration would reach the value.



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